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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,563	01/30/2004	Cesare Ronsisvalle	856063.761	5861

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/769,563	RONSISVALLE, CESARE	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-9 and 12-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *7,8 and 13-16* is/are allowed.

6)☐ Claim(s) *1,5,6,9,12 and 17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. On 11/9/05 Applicant argued that "Applicant's [6/29/05] Amendment did not require a new search because the amendments to the claims were subject matter taken from canceled dependent claims. In view of the foregoing, applicant submits that the Office Action mailed September 9, 2005, should have been a second, non-final office action." Applicant's argument is factually incorrect. Applicant's 6/29/05 amendment did in fact require a new search because each of claims 2,3, 5-9, and 12 presented claims to subject matter not previously searched. Applicant apparently intended to argue that if even a single claim (claim 1, in this instance) is to subject matter previously presented, and that claim is rejected using a new ground, the rejection cannot be made final. This is correct. See MPEP 706.07(b).

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 1,9,12,17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over MAJUMDAR (4,777,386) in view of BERTOLINI (5,631,588).

With regard to claim 1 Majumdar discloses an emitter switching configuration, comprising at least one bipolar transistor Q1 and a MOS transistor (part of base drive circuit 1– note that the MOS transistor is connected to bipolar transistor Q1 at B2, the base, and at E2, the emitter) having a common conduction terminal E2; and a Zener diode 15 inserted between a control terminal B2 of said bipolar transistor Q1 and said common conduction terminal E2, said Zener diode 15 having an anode terminal (note the figure to see which end is the anode and which is the cathode – the diode is clearly marked) connected to said control terminal B2 of said bipolar transistor Q1 and a cathode terminal (note the figure) connected to said common conduction terminal E2 of said bipolar transistor Q1, wherein said common conduction terminal E2 corresponds to an emitter terminal of said bipolar transistor Q1 and to a drain terminal of said MOS transistor (part of base drive circuit 1). Note figure 1 and column 3 lines 6-47 of Majumdar. Majumdar does not disclose that the Zener diode has a lower Zener voltage than a breakdown voltage of a junction between the base (control terminal) and emitter (common conduction terminal) of the bipolar transistor.

However, Bertolini discloses an emitter switch with output stage MOD M1, bipolar Q1, and Zener D2 attached so that the anode terminal of d2 is connected to the base of bipolar transistor Q1 at node "O" and the cathode of D2 is connected to said common conduction terminal E2 of said bipolar transistor Q1. Note figure 2A and column 5 lines

21-25 of Bertolini. Bertolini teaches that a MOS transistor M1 may be placed in an off condition causing the entire applied high-voltage overdriven supply node voltage Vb to reverse bias bipolar transistor Q1. However, according to Bertolini, when the base-emitter junction of transistor Q1 is reverse biased, Zener diode D2 is also reverse-biased (as may be seen from circuit 2a), so that the base-emitter voltage of transistor Q1 is limited to the reverse biased Zener voltage (chosen, note column 5 line 23, to be less than reverse bias emitter base breakdown voltage Vebo of transistor Q1) of Zener diode D2.

Therefore, it would have been obvious to a person having skill in the art to augment Majumdar's emitter switching configuration with the Zener diode having a lower Zener voltage than a breakdown voltage of a junction between the base and emitter of the bi-polar transistor such as taught by Bertolini in order to properly protect the bipolar transistor from reverse base-emitter breakdown when the MOS transistor is in an off condition to thus avoid the possible cost of replacing circuits in which reverse base-emitter breakdown of the bipolar transistor has caused unrepairable damage.

With regard to claims 9 and 12 Majumdar discloses an emitter switching circuit, comprising a bipolar transistor Q1 having a base-to-emitter device 15-16 coupled to a drain terminal of a MOS transistor (part of base drive circuit 1 – note that the MOS transistor is connected to bipolar transistor Q1 at B2, the base, and at E2, the emitter) and configured to prevent a breakdown condition of a body-drain junction of the MOS transistor (part of base drive circuit 1), the base-to-emitter device 15-16 comprising a Zener

diode 15 having an anode terminal connected to a base terminal of the bipolar transistor Q1 and a cathode terminal connected to an emitter terminal of the bipolar transistor Q1. Note figure 1 and column 3 lines 6-47 of Majumdar. Majumdar does not disclose that the Zener diode has a lower Zener voltage than a breakdown voltage of a junction between the base (control terminal) and emitter (common conduction terminal) of the bipolar transistor.

However, Bertolini discloses an emitter switch with output stage MOD M1, bipolar Q1, and Zener D2 attached so that the anode terminal of d2 is connected to the base of bipolar transistor Q1 at node "O" and the cathode of D2 is connected to said common conduction terminal E2 of said bipolar transistor Q1. Note figure 2A and column 5 lines 21-25 of Bertolini. Bertolini teaches that a MOS transistor M1 may be placed in an off condition causing the entire applied high-voltage overdriven supply node voltage Vb to reverse bias bipolar transistor Q1. However, according to Bertolini, when the base-emitter junction of transistor Q1 is reverse biased, Zener diode D2 is also reverse-biased (as may be seen from circuit 2a), so that the base-emitter voltage of transistor Q1 is limited to the reverse biased Zener voltage (chosen, note column 5 line 23, to be less than reverse bias emitter base breakdown voltage Vebo of transistor Q1) of Zener diode D2.

Therefore, it would have been obvious to a person having skill in the art to augment Majumdar's emitter switching configuration with the Zener diode having a lower Zener voltage than a breakdown voltage of a junction between the base and emitter of the bi-

polar transistor such as taught by Bertolini in order to properly protect the bipolar transistor from reverse base-emitter breakdown when the MOS transistor is in an off condition to thus avoid the possible cost of replacing circuits in which reverse base-emitter breakdown of the bipolar transistor has caused unrepairable damage.

With regard to claims 17 and 18 Majumdar discloses a circuit, comprising at least one bipolar transistor Q1 having a collector terminal, an emitter terminal (following usual practice Majumdar marks his emitter with a small arrow and leaves his collector unmarked), and a base terminal; at least one MOS transistor (part of base drive circuit 1), having a gate terminal (gate, source, and drain terminals are readily discernible from the otherwise unmarked circuit diagram), a first drain terminal, and a second (usual practice is to call the second terminal a "source") terminal, the drain terminal of the MOS transistor coupled to the emitter terminal of the bipolar transistor Q1 at a first node; and a Zener diode 15 having an anode terminal (Majumdar's circuit marks the anode and cathode of Zener diode 15 in the manner accepted by those having skill in the art of drawing and reading circuit diagrams) coupled to the base terminal of the bipolar transistor Q1 and a cathode terminal coupled to the first node. Note figure 1 and column 3 lines 6-47 of Majumdar. Majumdar does not disclose that the Zener diode has a lower Zener voltage than a breakdown voltage of a junction between the base (control terminal) and emitter (common conduction terminal) of the bipolar transistor.

However, Bertolini discloses an emitter switch with output stage MOD M1, bipolar Q1, and Zener D2 attached so that the anode terminal of d2 is connected to the base of

bipolar transistor Q1 at node "O" and the cathode of D2 is connected to said common conduction terminal E2 of said bipolar transistor Q1 at node "X." Note figure 2A and column 5 lines 21-25 of Bertolini. Bertolini teaches that a MOS transistor M1 may be placed in an off condition causing the entire applied high-voltage overdriven supply node voltage Vb to reverse bias bipolar transistor Q1. However, according to Bertolini, when the base-emitter junction of transistor Q1 is reverse biased, Zener diode D2 is also reverse-biased (as may be seen from circuit 2a), so that the base-emitter voltage of transistor Q1 is limited to the reverse biased Zener voltage (chosen, note column 5 line 23, to be less than reverse bias emitter base breakdown voltage Vebo of transistor Q1) of Zener diode D2.

Therefore, it would have been obvious to a person having skill in the art to augment Majumdar's emitter switching configuration with the Zener diode having a lower Zener voltage than a breakdown voltage of a junction between the base and emitter of the bipolar transistor such as taught by Bertolini in order to properly protect the bipolar transistor from reverse base-emitter breakdown when the MOS transistor is in an off condition to thus avoid the possible cost of replacing circuits in which reverse base-emitter breakdown of the bipolar transistor has caused unrepairable damage.

B. Claims 5,6, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over MAJUMDAR (4,777,386) in view of BERTOLINI (5,631,588), as applied to claims 1 and 17 above, and further in view of LUONI et al.

With regard to claims 5 and 6 Majumdar and Bertolini suggest a device having all the limitations of claims 5 and 6 except that the MOS transistor be a vertical low breakdown double diffusion type transistor. Note figure 1 and column 3 lines 6-47 of Majumdar and figure 2A and column 5 lines 21-25 of Bertolini.

However, Luoni et al. discloses an emitter switch having a MOS transistor Tm having a low breakdown voltage, and said MOS transistor Tm is of the vertical double-diffusion type. Note figure 2 and column 3 lines 29-60 of Luoni et al. Therefore, it would have been obvious to a person having skill in the art to replace the MOS transistor of Majumdar and Bertolini's device with the vertical double-diffusion type MOS transistor Tm having a low breakdown voltage such as taught by Luoni et al. in order to reduce the cost of making the MOS transistor by making it small and cheap and easily broken down, as well as conserving wafer space by mounting the MOS transistor vertically.

With regard to claim 19 Majumdar and Bertolini suggest a device having all the limitations of claims 5 and 6 except that the MOS transistor be a vertical double diffusion type transistor. Note figure 1 and column 3 lines 6-47 of Majumdar and figure 2A and column 5 lines 21-25 of Bertolini.

However, Luoni et al. discloses an emitter switch having a MOS transistor Tm of the vertical double-diffusion type. Note figure 2 and column 3 lines 29-60 of Luoni et al. Therefore, it would have been obvious to a person having skill in the art to replace the MOS transistor of Majumdar and Bertolini's device with the MOS transistor of the verti-

cal double-diffusion type such as taught by Luoni et al. in order to reduce the cost of making the MOS transistor by conserving wafer space by mounting the MOS transistor vertically.

Response to Arguments

3. Applicant's arguments with respect to claims 1,5,6,9,12, and 17-19 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

4. Claims 7,8, and 13-16 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as an emitter switching configuration, comprising at least one substrate in which are formed second wells of first conductivity type, adjacent to first wells of second conductivity type and in contact with said first wells and with a second buried layer to define a Zener diode parallel to a junction defined by a first buried layer and said second buried layer with an anode of the Zener diode coupled to a control terminal of a bipolar transistor and a cathode coupled to a common conduction terminal where the emitter of the bipolar transistor is connected to the drain of a MOSFET, as recited in claims 7 and 13.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

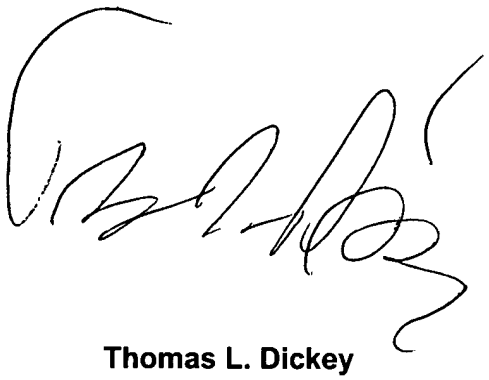
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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Art Unit 2826
11/05